

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/473,263	12/27/1999	LARRY D. KINSMAN	3399.2US	9776	
75	590 09/23/2002				
BRICK G POWER			EXAMINER		
TRASK BRITT & ROSSA			CRUZ, LOURDES C		
P O BOX 2550			 ,		
SALT LAKE C	CITY, UT 84110		ART UNIT	PAPER NUMBER	
			2827		

DATE MAILED: 09/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

					ala			
		Application	n No.	plicant(s)				
Office Action Summary		09/473,263	3	KINSMAN, LARRY D.				
		Examiner		Art Unit				
		Lourdes C.		2827				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed								
after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status 1)⊠	Responsive to communication(s) filed on 7-	22.02						
2a)□		·23-02 . This action is r	non-final					
3)□	/ —			prosecution as to the	merits is			
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims								
4)⊠ Claim(s) <u>1-6 and 8-24</u> is/are pending in the application.								
4a) Of the above claim(s) is/are withdrawn from consideration.								
5) Claim(s) is/are allowed.								
6)⊠ Claim(s) <u>1-6,8-24</u> is/are rejected.								
7)	7) Claim(s) is/are objected to.							
-	Claim(s) are subject to restriction and	l/or election re	quirement.					
Application Papers								
9) The specification is objected to by the Examiner.								
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.								
If approved, corrected drawings are required in reply to this Office action.								
12) The oath or declaration is objected to by the Examiner.								
Priority under 35 U.S.C. §§ 119 and 120								
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).								
a)	☐ All b)☐ Some * c)☐ None of:							
1. Certified copies of the priority documents have been received.								
2. Certified copies of the priority documents have been received in Application No								
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).								
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.								
Attachment(s)								
1) Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449) Paper No(s)			mary (PTO-413) Paper No(s nal Patent Application (PTC				

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 8-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Beilstein, Jr. et al. (US 5786628).

Beilstein teaches a vertical surface mount semiconductor device, comprising:

A semiconductor device 13; bond pads (15) on a surface of said device and adjacent an edge thereof and arranged substantially in line (since bond pads are defined as being "proximate said edge", they must be substantially in line); bumps 29 disposed adjacent selected bond pads, each bump configured to form a conductive joint between one of said selected bond pads and a corresponding terminal 53 of a substrate 41.

See that Beilstein also teaches:

- Bumps adjacent to the bond pads (Claims 2,12 and 20)
- A support (to the left of 13) layer 19 (Claims 3,4-6,10,11,15-17, and
 21-23). See page 8 of the disclosure, lines 4-5.
- Joints 27 adjacent said bond pads (Claim 14)
- A Semiconductor device laminated to an adjacent one (Claims 8,18 and 24).

Regarding Claim 19, see that all the structural limitations recited in the claim have been addressed above. However, the claim also recites an intended use. See In re Pearson 181 USPQ 641 (CCPA) which makes clear that terms merely setting forth intended use for, or a property inherent in, an otherwise old composition do not differentiate claimed composition from those known to prior art. See also, In re Swinehart [169 USPQ 226] (CCPA 1971) which makes clear that mere recitation of a newly discovered function or property, inherently possessed by things in prior art, does not cause claim drawn to those things to distinguish over prior art.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-21 of U.S. Patent No. 6140696. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Although the claims of the instant Application and the claims of Patent No. 6140696 are not the same, the subject matter there between is identical. That is, the semiconductor device defined in the instant Application inherently includes "an edge, an active surface, and a back side opposite said active surface". Also, although the present claims recite "substantially in line", this language is inherent in the claims since bond pads are defined as being "proximate said edge", meaning they must be substantially in line. Furthermore, if they were not "substantially in line" the semiconductor device could not be a vertical surface.

Response to Arguments

Although Applicant's arguments filed 7-23-02 regarding the previous double patenting rejection were found persuasive (see new double patenting rejection above), the following remarks and arguments have been fully considered but they are not persuasive:

- "It is not clear whether the Office has taken the position that it is the I/O pads of the chips 13 described in Beilstein that are the "bond pads"... or that "bond pads" are the contacts 27..."
- Beilstein neither expressly nor inherently describes that conductive bumps may be disposed adjacent the I/O pads of the chips 13 of the module 11 described therein, or that such conductive bumps could be configured to form a conductive joint between the I/O pad and a corresponding terminal of a substrate

- The conductive joint 29 of Beilstein is positioned at a location that is remote from its corresponding I/O pad, not adjacent thereto
- Beilstein does not describe I/O pads arranged substantially in-line
- Conductive traces and bond pads are different types of structures
- Beilstein does not disclose bond pads "within the meaning of either independent claim..."
- Contacts 27 are not located on the surfaces of the chips 13, but
 rather on a side surface of the module 11
- Beilstein fails to teach a support footing
- Beilstein does not teach joints directly between selected bond pads and their corresponding terminals

The **above** arguments and remarks are **not persuasive** for the following reasons:

- The examiner has clearly pointed out on the previous Office action that element 15 of Beilstein was the element reading on "bond pads"
- Beilstein clearly teaches bumps 29 adjacent I/O pads of the chip 13, and this bumps are conductive (Col. 11, line 18) and do connect the chips to the traces in 41 (Col. 11, lines 15+)
- The examiner is puzzled by applicant's remarks, specifically because applicant bases his arguments by changing the reference numbers of Beilstein as pointed out by the examiner in the previous

Office Action, with his own interpretation of Beilstein. See that while Applicant argues "the conductive joints 29", the examiner specifically pointed out that she was reading member 27 of Beilstein to be the one reading on the "conductive joint" of the Applicant. Nevertheless, the examiner will like to point out that applicant's argument regarding "remote to" and "adjacent to" are not persuasive for these terms are terms of relativity and are subjected to individual interpretation, therefore defining no specific distance.

- Beilstein discloses pads arranged substantially in-line, because "substantially in line" is inherent in the claims since bond pads are defined as being "proximate said edge", meaning they must be substantially in line. Furthermore, if they were not "substantially in line" the semiconductor device could not be a vertical surface.
- Moreover, labels, statements of intended use, or functional language such as we have here in "bond pads" does not structurally distinguish the claim over the prior art which shows a structure that may likewise be labeled, used or function as a bond pad rather than a "conductive trace". See *In re Pearson* 181 USPQ 641, Ex parte Minks 169 USPQ 120, and *In re Swinwhart* 169 USPQ 226.

- Contacts 27 are located on the surfaces of the chips 13, and on a side surface of the module 11. While 27 might not be directly on 13, it is still on 13.
- Again, the examiner is puzzled by Applicant's arguments, specifically by "contact pads 27..." since the examiner clearly pointed out 15 as reading on applicant's claimed contact pads. However, "Contact pads 27" of module 11 are adjacent an edge of any chip, as clearly shown by Beilstein. See that directly adjacent has not been claimed, nor has applicant recited any language that will prevent any other layer in between the claimed structures.
- Beilstein clearly teaches support footing 19

١.

 Beilstein teaches joints 27 directly between bond pads 15 and corresponding terminals in the substrate 41

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See that Choi (US 6198164) teaches vertically mounted semiconductor devices laminated to one another using a heat dissipating material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 707-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lourdes C. Cruz Examiner Art Unit 2827

Lourdes Cruz

September 17, 2002

KAMAND CUNEO

SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800